

1Mb ~ 16Mb PPI MRAM

- **S3R1016V1M**
- **S3R2016V1M**
- **S3R4016V1M**
- **S3R8016V1M**
- **S3R1616V1M**
- **S3R1008V1M**
- **S3R2008V1M**
- **S3R4008V1M**
- **S3R8008V1M**
- **S3R1608V1M**

Parallel Peripheral Interface MRAM 3.3V

Revision 0.2

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Feature

- Interface
 - Parallel Asynchronous and Page Mode Interface
- Page Mode Read Access
 - Interpage read access : 70ns
 - Intrapage read access : 15ns
- Page Mode Write Access
 - Interpage write access : 320ns
 - Intrapage write access : 15ns
- Page Size
 - x16 I/O Mode : 4-word page size
 - x8 I/O Mode : 8-word page size
- Low Power Consumption
 - Read current : 15mA
 - Write current : 15mA
 - Standby current : 350uA
- Data Byte Control(x16 I/O Mode)
 - \overline{LB} : DQ₇~DQ₀, \overline{UB} : DQ₁₅~DQ₈
- Memory cell : STT-MRAM
 - nonvolatile
- Density
 - 16Mb, 8Mb, 4Mb, 2Mb and 1Mb
- Data Integrity : No external ECC required
- Data Endurance
 - Unlimited read cycle
 - 10¹⁴ write cycles
- Data Retention
 - 10 years at 85°C
- Single Power Supply Operation
 - S3RxxxxV1M: 2.70V~3.60V
- Operating Temperature Range
 - Industrial Temperature : -40°C to 85°C
- RoHS compliant packages
 - 44TSOP2 (10mm x 18mm)
 - 48FBGA (6mm x 8mm)
 - 54TSOP2 (10mm x 22mm)

Performance

Operation		Symbol	Typical Values	Units
Interpage Read Cycle Time		t _{RC}	70(Max.)	ns
Intrapage Read Cycle Time		t _{PRC}	15(Max.)	ns
Interpage Write Cycle Time		t _{WC}	320(Max.)	ns
Intrapage Write Cycle Time		t _{PWC}	15(Max.)	ns
Standby Current	16Mb	I _{SB}	350	uA
	1Mb~8Mb		235	
Interpage Read Current		I _{CCR}	15	mA
Intrapage Read Current		I _{CCRP}	15	mA
Interpage Write Current		I _{CCW}	15	mA
Intrapage Write Current		I _{CCWP}	15	mA

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General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM).

Data is always non-volatile and the device can replace FRAM, low-power SRAM or nvSRAM with same functionality and help to simplify system design. Due to the non-volatility and virtually unlimited endurance characteristics of STT-MRAM, it is suited for code storage, data logging, backup memory and working memory in industrial designs.

It is offered in density ranging from 1Mbit to 16Mbit. It is a fully random-access memory with parallel asynchronous interface. x16 or x8 I/O mode are supported. And x16 I/O mode allows that lower and upper byte access by data byte control (\overline{LB} , \overline{UB}).

It supports the asynchronous page mode function to enhance the read and write performance. The page size of x16 I/O mode and x8 I/O mode is 4 words and 8 words.

The S3Rxx16V1M is packaged in industrial standard 44TSOP2, 54TSOP2 and 48FBGA.

The S3Rxx08V1M is packaged in industrial standard 44TSOP2 and 48FBGA. These packages are compatible with similar low-power volatile and non-volatile products.

The device is offered with industrial (-40°C to 85°C) operating temperature range.

Pin Description – x16 I/O mode

Figure 1 : Functional Block Diagram – x16 I/O mode

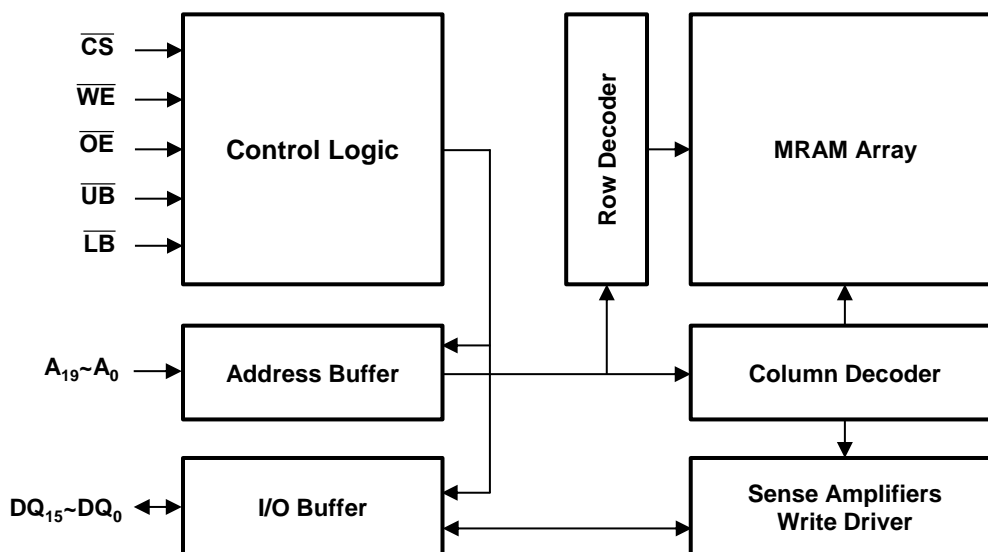


Table 1 : Pin Description – x16 I/O mode

Pin	Type	Description
\overline{CS}	Input	Chip Select: When \overline{CS} is driven Low, read or write operation are initiated. When \overline{CS} is driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. \overline{CS} should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
\overline{WE}	Input	Write Enable: When \overline{CS} and \overline{WE} are driven Low, write operation is initiated. The rising edge of \overline{CS} causes the device to transfer the data to memory array. The rising edge of \overline{WE} latches the input data. And, the falling edge of \overline{WE} latches a new page address for write cycles.
\overline{OE}	Input	Output Enable
\overline{LB}	Input	Lower Byte Control: $DQ_7 \sim DQ_0$
\overline{UB}	Input	Upper Byte Control: $DQ_{15} \sim DQ_8$
$A_{19} \sim A_0$	Input	Address The LSB address $A_1 \sim A_0$ are used for page mode read and write operation.
$DQ_{15} \sim DQ_0$	Bidirectional	Data Input/Outputs
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use : DNU's must be left unconnected.

Pin Description – x8 I/O mode

Figure 2 : Functional Block Diagram – x8 I/O mode

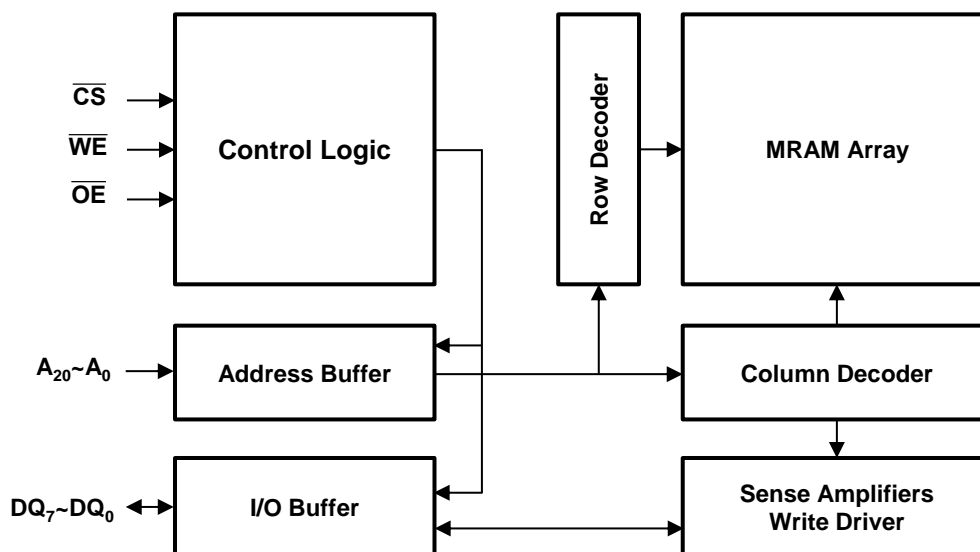
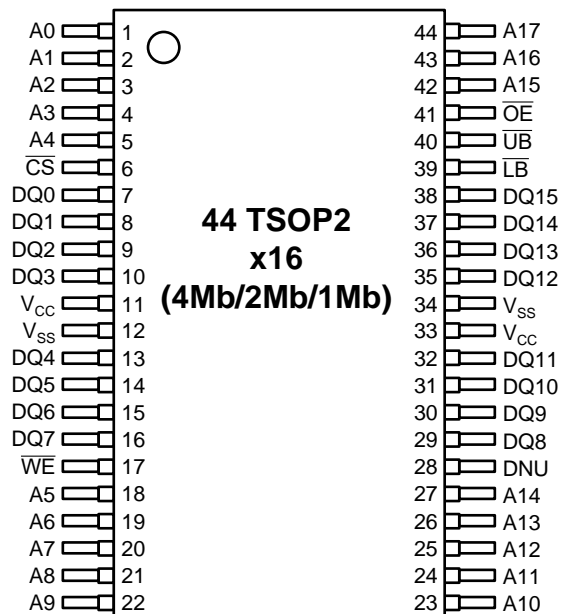
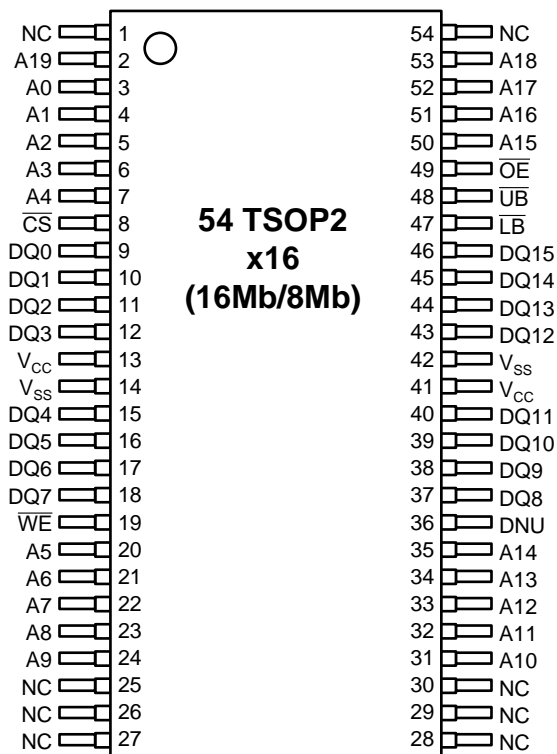


Table 2 : Pin Description – x8 I/O mode

Pin	Type	Description
\overline{CS}	Input	Chip Select: When \overline{CS} is driven Low, read or write operation are initiated. When \overline{CS} is driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. \overline{CS} should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
\overline{WE}	Input	Write Enable: When \overline{CS} and \overline{WE} are driven Low, write operation is initiated. The rising edge of \overline{CS} causes the device to transfer the data to memory array. The rising edge of \overline{WE} latches the input data. And, the falling edge of \overline{WE} latches a new page address for write cycles.
\overline{OE}	Input	Output Enable
$A_{20} \sim A_0$	Input	Address The LSB address $A_2 \sim A_0$ are used for page mode read and write operation.
$DQ_7 \sim DQ_0$	Bidirectional	Data Input/Outputs
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use : DNUs must be left unconnected.

Package Pin Configuration – x16 I/O mode



48 Ball FBGA(16Mb~1Mb, x16)

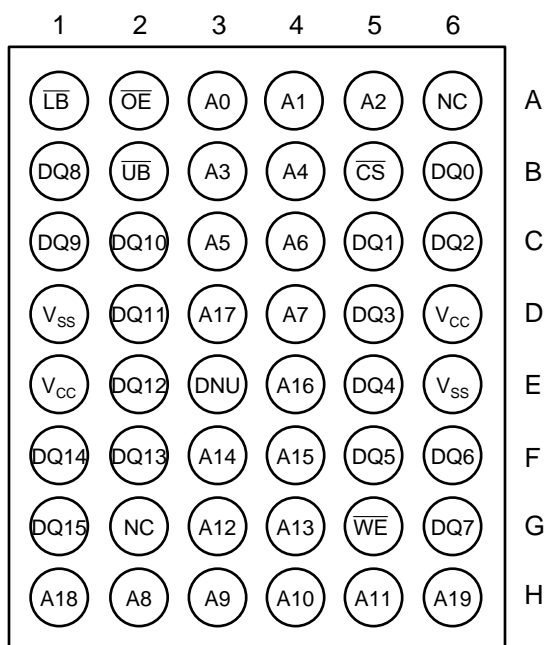


Table 3 : DNU Pin Description – x16 I/O mode

Package	Density	Part Number	DNU pin
54 TSOP2	All	All	#36
	8Mb	S3R8016V1M	#2(A19)
44 TSOP2	All	All	#28
	2Mb	S3R2016V1M	#44(A17)
	1Mb	S3R1016V1M	#44(A17),#43(A16)
48 FBGA	All	All	E3
	8Mb	S3R8016V1M	H6(A19)
	4Mb	S3R4016V1M	H6(A19),H1(A18)
	2Mb	S3R2016V1M	H6(A19),H1(A18), D3(A17)
	1Mb	S3R1016V1M	H6(A19),H1(A18), D3(A17),E4(A16)

Package Pin Configuration – x8 I/O mode

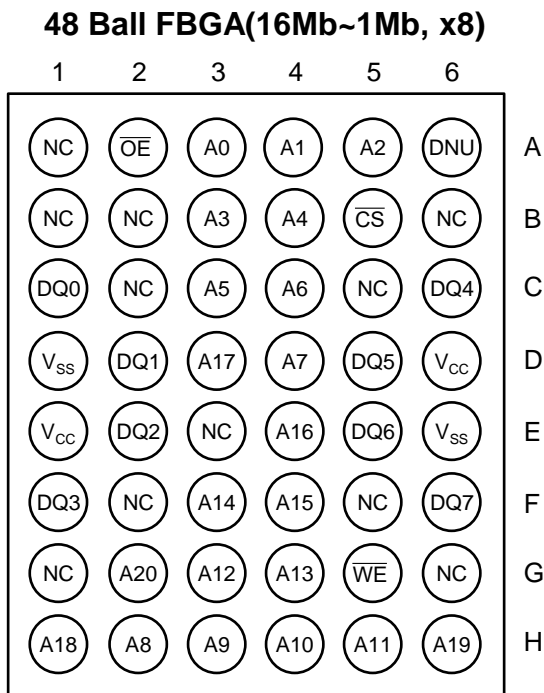
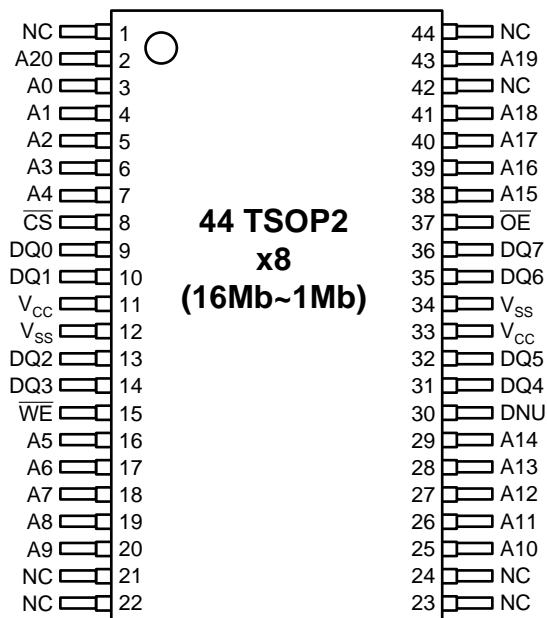


Table 4 : DNU Pin Description – x8 I/O mode

Package	Density	Part Number	DNU pin
44 TSOP2	All	All	#30
	8Mb	S3R8008V1M	#2(A20)
	4Mb	S3R4008V1M	#2(A20),#43(A19)
	2Mb	S3R2008V1M	#2(A20),#43(A19),#41(A18)
	1Mb	S3R1008V1M	#2(A20),#43(A19),#41(A18),#40(A17)
48 FBGA	All	All	A6
	8Mb	S3R8008V1M	G2(A20)
	4Mb	S3R4008V1M	G2(A20),H6(A19)
	2Mb	S3R2008V1M	G2(A20),H6(A19),H1(A18)
	1Mb	S3R1008V1M	G2(A20),H6(A19),H1(A18),D3(A17)

Functional Description

Functional Description - x16 I/O mode

Table 5 : Functional Description - x16 I/O mode

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	DQ ₇ ~DQ ₀	DQ ₁₅ ~DQ ₈	Modes	Supply Current
H	X	X	X	X	High-Z	High-Z	Not Selected	I _{SB}
L	H	H	X	X	High-Z	High-Z	Output disable	I _{CCR}
L	H	L	H	H	High-Z	High-Z	Output disable	I _{CCR}
L	H	L	L	H	Dout	High-Z	Lower Byte Read	I _{CCR}
L	H	L	H	L	High-Z	Dout	Upper Byte Read	I _{CCR}
L	H	L	L	L	Dout	Dout	Word Read	I _{CCR}
L	L	X	H	H	High-Z	High-Z	Input disable	I _{CCW}
L	L	X	L	H	Din	High-Z	Lower Byte Write	I _{CCW}
L	L	X	H	L	High-Z	Din	Upper Byte Write	I _{CCW}
L	L	X	L	L	Din	Din	Word Write	I _{CCW}

Functional Description - x8 I/O mode

Table 6 : Functional Description - x8 I/O mode

\overline{CS}	\overline{WE}	\overline{OE}	DQ ₇ ~DQ ₀	Modes	Supply Current
H	X	X	High-Z	Not Selected	I _{SB}
L	H	H	High-Z	Output disable	I _{CCR}
L	H	L	Dout	Word Read	I _{CCR}
L	L	X	Din	Word Write	I _{CCW}

Notes:

1. H = High, L = Low, X = don't care, High-Z : high impedance

Address Pin

Table 7 : Address Pin

Density	Address Pin x16 I/O mode	Address Pin x8 I/O mode
16Mb	A[19:0]	A[20:0]
8Mb	A[18:0]	A[19:0]
4Mb	A[17:0]	A[18:0]
2Mb	A[16:0]	A[17:0]
1Mb	A[15:0]	A[16:0]

Parameter	x16 I/O mode	x8 I/O mode
Page Address	A ₁ ~A ₀	A ₂ ~A ₀

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 8 : Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage on Vcc Supply Relative to VSS	-0.5	3.8	V
Voltage on Any Pin relative to VSS	-0.5	3.8	V
Storage Temperature	-55	150	°C
Operating Ambient Temperature	-40	85	°C
ESD HBM (Human Body Model)	≥ 2000 V		V
ESD CDM (Charged Device Model)	≥ 500 V		V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles - Peak temperature ≤ 260°C - The time above 255°C ≤ 30 seconds - Reflow cycles ≤ 3 times		

Endurance, Retention and Magnetic Immunity

Table 9 : Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Units
Write Endurance	-25°C	10 ¹⁴	-	Cycles/page
Data Retention	85°C	10	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

Recommended Operating Conditions

Table 10 : Recommended Operating Conditions

Parameter / Condition	Min.	Typ.	Max.	Units
Operating Temperature	-40	25	85	°C
Vcc Supply Voltage	2.7	3.3	3.6	V
Vss Supply Voltage	0.0	0.0	0.0	V

Pin Capacitance

Table 11 : Pin Capacitance

Parameter	Conditions	Typ.	Max.	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V _{IN} = 0V	-	4	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V _{IO} = 0V	-	6	pF

* Capacitance is sampled and not 100% tested

AC Test Condition

Table 12 : AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V _{CC}
Input rise and fall times	1ns/1V
Input and output measurement timing levels	V _{CC} /2
Output Load	CL = 30pF

DC Characteristics

Table 13 : DC Characteristics

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	-2	-	+2	uA	
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} = V _{SS} to V _{CC}	-2	-	+2	uA	
Read Current	Random	I _{CCR}	V _{CC} (max), I _{OUT} =0mA	-	15	TBD	mA
	Page mode	I _{CCRP}	V _{CC} (max), I _{OUT} =0mA	-	15	TBD	mA
Write Current	Random	I _{CCW}	V _{CC} (max)	-	15	TBD	mA
	Page mode	I _{CCWP}	V _{CC} (max)	-	15	TBD	mA
Standby Current	16Mb	I _{SB}	V _{CC} (max), $\overline{CS}\leq V_{CC}-0.2V$	-	350	TBD	uA
	1Mb~8Mb			-	235	TBD	uA
Input High Voltage	V _{IH}	-	0.7xV _{CC}	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL}	-	-0.2	-	0.2xV _{CC}	V	
Output High Voltage	V _{OH}	I _{OH} =-1mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} =2mA	-	-	0.4	V	

AC Timing Parameters

Table 14 : Read AC Timing Parameter

Parameter	Symbol	Min.	Max.	Units
Read Cycle Time (Interpage)	t_{RC}	70	-	ns
Page Read Cycle Time (Intrapage)	t_{PRC}	15	-	ns
\overline{CS} Read Active Time	t_{RCA}	65	-	ns
\overline{CS} Falling to Valid Output Time	t_{CO}	-	65	ns
Address Access Time ²⁾	t_{AA}	-	80	ns
Page Address Access Time	t_{PAA}	-	15	ns
\overline{CS} Rising to Output Hold Time	t_{COH}	3	-	ns
Address change to Output Hold Time ²⁾	t_{OH}	30	-	ns
Page address change to Output Hold Time	t_{POH}	5	-	ns
\overline{OE} Falling to Valid Output Time	t_{OE}	-	15	ns
\overline{UB} , \overline{LB} Falling to Valid Output Time ¹⁾	t_{BA}	-	15	ns
\overline{CS} Rising to High-Z Output Time	t_{CHZ}	-	8	ns
\overline{OE} Rising to High-Z Output Time	t_{OHZ}	-	8	ns
\overline{UB} , \overline{LB} Rising to High-Z Output Time ¹⁾	t_{BHZ}	-	8	ns
Address Transition to \overline{CS} falling Time ²⁾	t_{CAS}	0	-	ns
\overline{CS} Rising to Address Transition Time ²⁾	t_{CAH}	0	-	ns
\overline{WE} Rising to \overline{CS} Falling Time	t_{WES}	0	-	ns
\overline{CS} Rising to \overline{WE} Falling Time	t_{WEH}	0	-	ns
\overline{CS} High Time for Read End	t_{CSDR}	5	-	ns
Address Transition Interval Time	t_{AX}	-	5	ns

*** Note:**

1. Those parameters are applied for x16 I/O mode only.
2. Address except for page address

AC Timing Parameters

Table 15 : Write AC Timing Parameter

Parameters	Symbol	Min	Max	Unit
Write Cycle Time (Interpage)	t_{WC}	320	-	ns
\overline{CS} Write Active Time ³⁾	t_{WCA}	20	-	ns
\overline{CS} Falling to End of Write Time	t_{CW}	20	-	ns
Page Write Cycle Time (Intrapage)	t_{PWC}	15	-	ns
\overline{WE} Falling to End of Write (invalid output does not appear)	t_{WP}	10	-	ns
\overline{WE} Falling to End of Write (invalid output appears)	t_{WP1}	20	-	ns
\overline{UB} , \overline{LB} Falling to End of Write Time ¹⁾	t_{BW}	10	-	ns
\overline{WE} Falling to Output High-Z Time	t_{WHZ}	-	8	ns
Valid Input Data to End of Write Time	t_{DS}	8	-	ns
End of Write to Valid Input Data Time	t_{DH}	0	-	ns
Address Transition Time to \overline{CS} falling ²⁾	t_{CAS}	0	-	ns
\overline{CS} Rising to Address Transition Time ²⁾	t_{CAH}	0	-	ns
Page Address Transition to \overline{WE} falling Time	t_{PAS}	0	-	ns
\overline{WE} falling to Page Address Transition Time	t_{PAH}	10	-	ns
\overline{WE} High Time for Page Write	t_{PWH}	3	-	ns
\overline{CS} High Time for Write End ³⁾	t_{CSDW}	250	-	ns

*** Note:**

1. Those parameters are applied for x16 I/O mode only.
2. Address except for page address
3. $t_{WCA} + t_{CSDW} \geq t_{WC}$

Power On/Off Sequence

- When power-up, power-down or power-loss, \overline{CS} must follow V_{cc} to provide data protection.
- It is recommended that \overline{CS} must follow V_{cc} when V_{cc} is below $V_{cc}(\text{minimum})$ and during t_{PU} .
- A 10K Ω pull-up resistor between V_{cc} and \overline{CS} pin is recommended.
- Normal operation must start after t_{PU} .

Figure 3 : Power-Up/Down Behavior

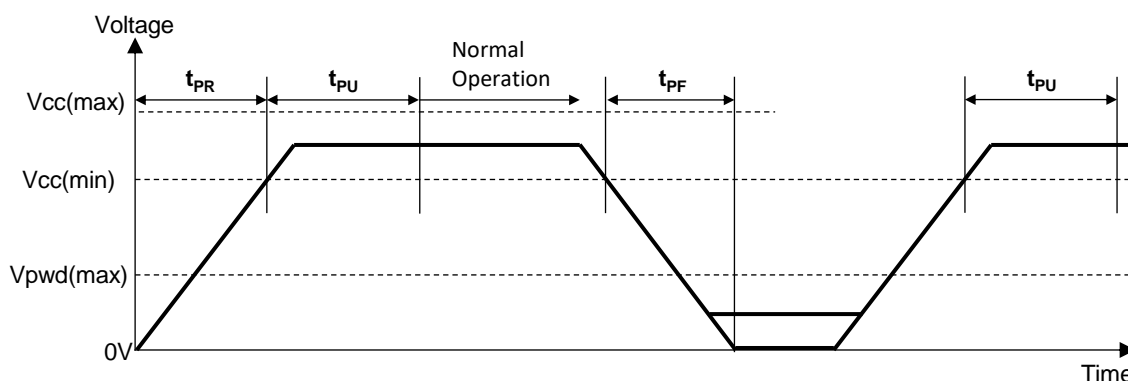


Table 16 : Power-Up/Down Timing

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	2.7	3.6	V
Vcc rising time	$t_{PR}^{(1)}$	30	-	$\mu\text{s}/\text{V}$
Vcc falling time	$t_{PF}^{(1)}$	30	-	$\mu\text{s}/\text{V}$
Vcc(min) to \overline{CS} Low (first instruction) time	$t_{PU}^{(1)}$	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	$V_{PWD}^{(1)}$	-	1.6	V

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

Device Operation

Read Operation : Interpage

Read operation is initiated when \overline{CS} goes to low and \overline{WE} is high. The falling edge of \overline{CS} latches the address and starts to read data from memory array. The output data are available after t_{CO} . The minimum random read cycle time is t_{RC} . The data remains in High-Z until the valid data is output.

Figure 4 : Timing Waveform of Read Cycle : x16 I/O mode

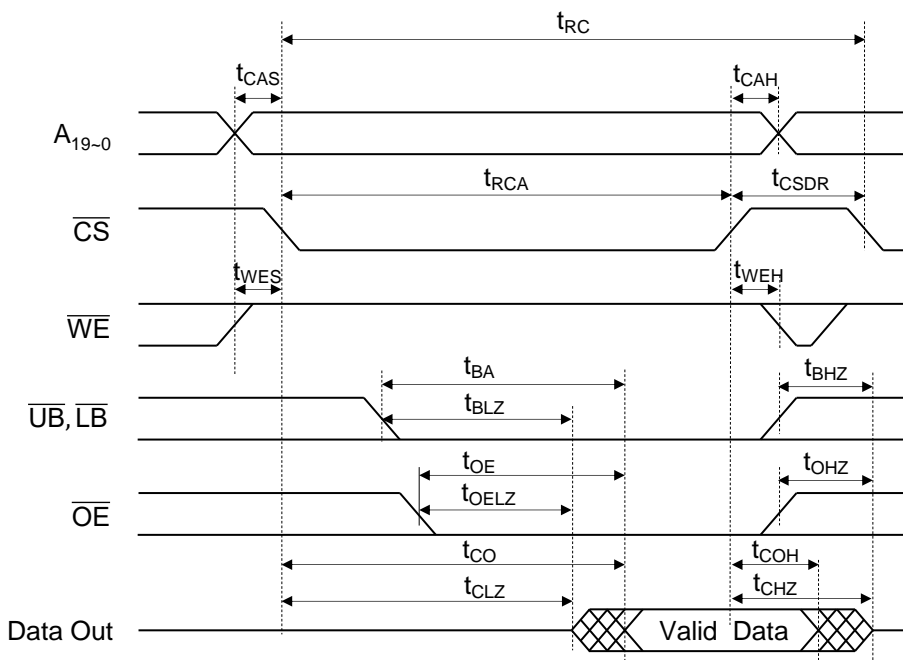
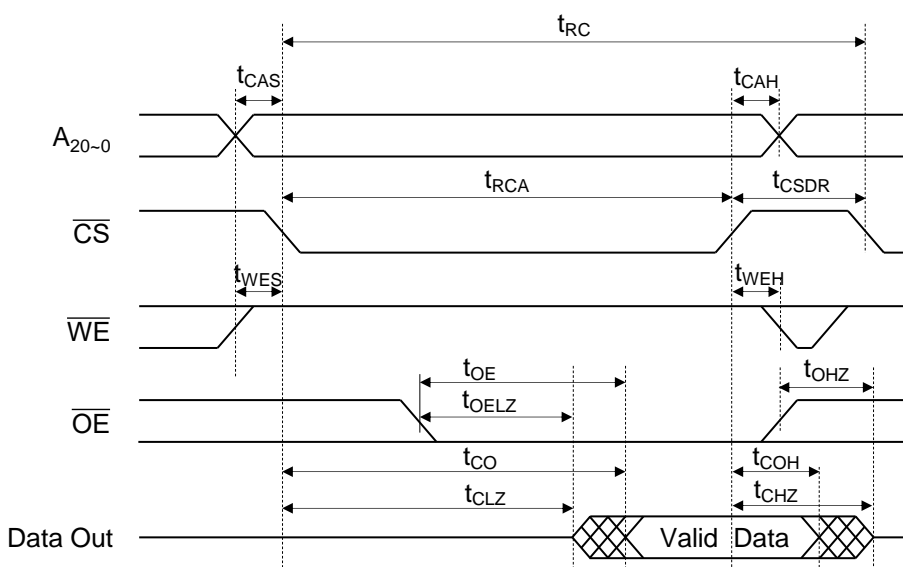


Figure 5 : Timing Waveform of Read Cycle : x8 I/O mode



Page Mode Read Operation : Intrapage

The device supports the page mode read function to enhance the read performance. It reads a page data from memory array and latches the data into an internal page buffer. The first data is output after t_{CO} . When the next page address is input, subsequent data is output from the page buffer after t_{PAA} . The sequence and length of page address are not restricted. For example, the sequence A2-A0-A1 is available.

Parameter	x16 I/O mode	x8 I/O mode
Page Address	A ₁ ~A ₀	A ₂ ~A ₀
Page size	4-word (8-bytes)	8-word (8-bytes)

Figure 6 : Timing Waveform of Page Mode Read Cycle : x16 I/O mode

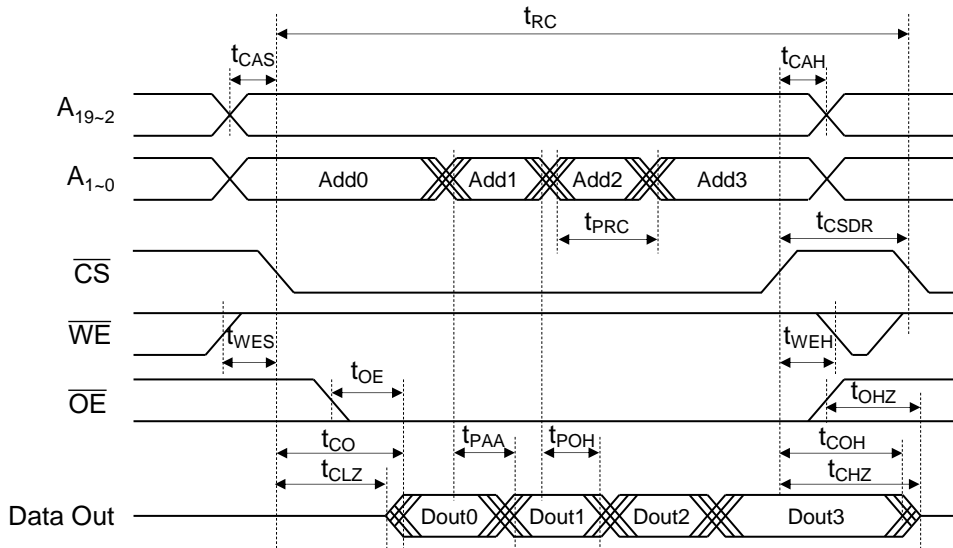
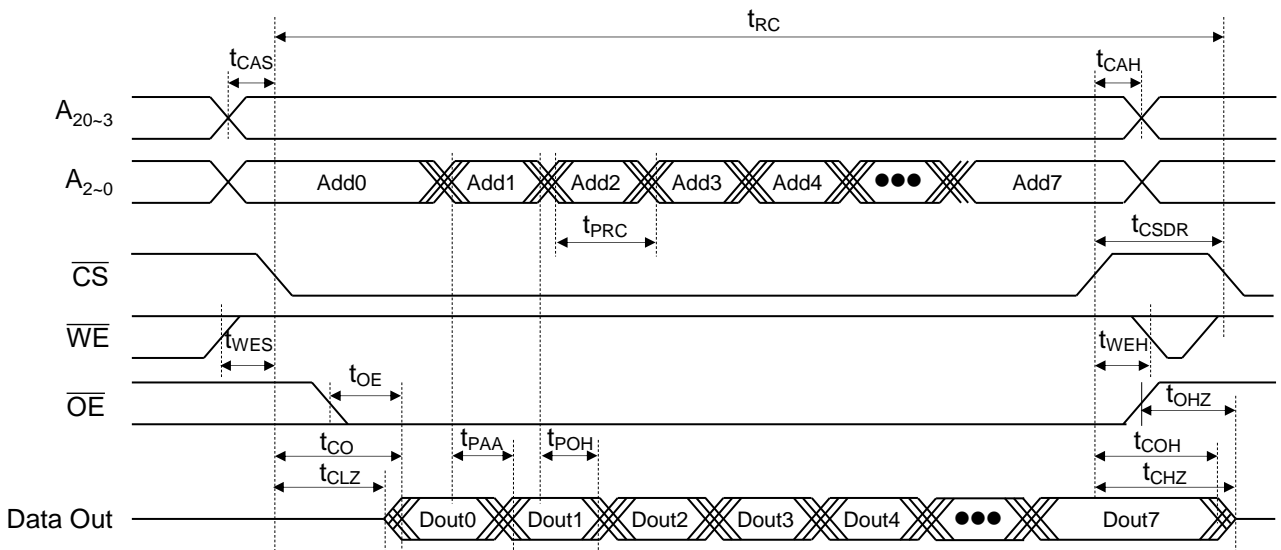


Figure 7 : Timing Waveform of Page Mode Read Cycle : x8 I/O mode



Address Access Read Operation

During \overline{CS} is low and \overline{WE} is high, if a random address (except for the page address) are changed, the device reads a page data from memory array of a new address and latches the data into an internal page buffer. The first data is output after t_{AA} . When the next page address is input, subsequent data is output from the page buffer after t_{PAA} . The random address transition time should not exceed t_{AX} .

Figure 8 : Timing Waveform of Address Access Read Cycle : x16 I/O mode

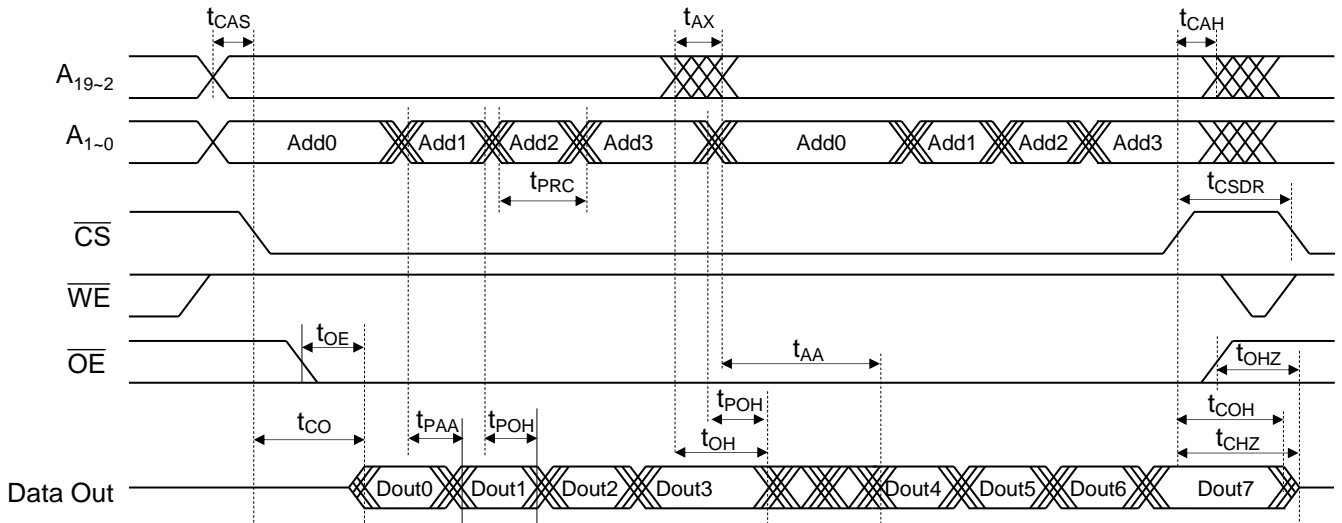
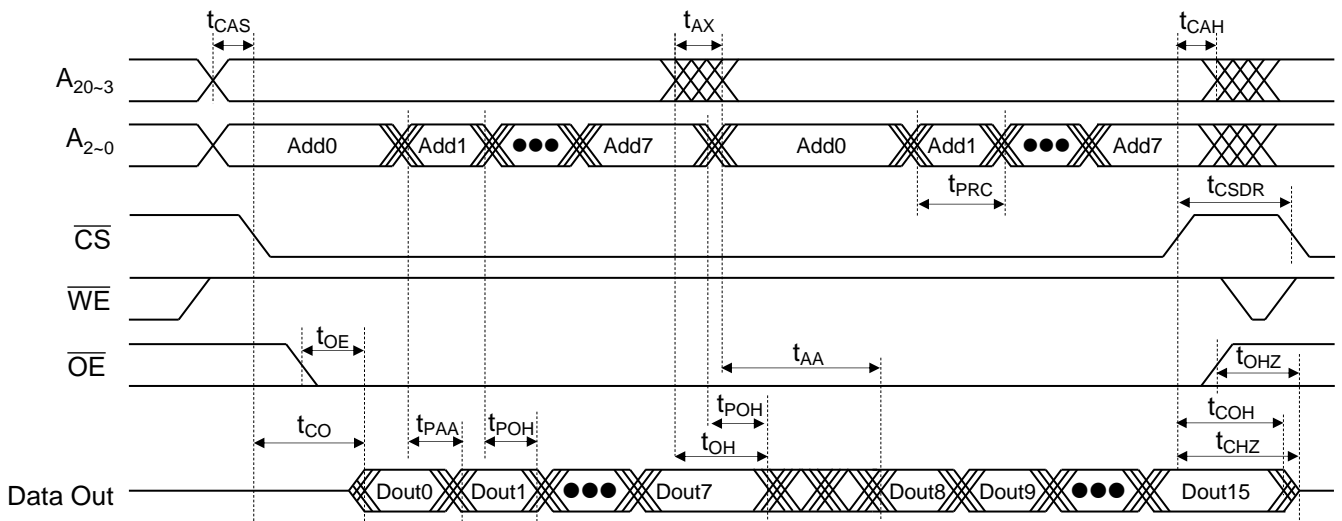


Figure 9 : Timing Waveform of Address Access Read Cycle : x8 I/O mode



Write Operation (\overline{WE} control) : Interpage

Write operation is initiated when \overline{WE} goes to low and \overline{CS} is low.

The device latches address on the falling edge of \overline{CS} . It latches the lower byte data on the rising edge of \overline{WE} or \overline{LB} and the upper byte data on the rising edge of \overline{WE} or \overline{UB} for x16 I/O mode.

It latches the data on the rising edge of \overline{WE} for x8 I/O mode.

The rising edge of \overline{CS} causes the device to transfer the input data to memory array.

Figure 10 : Timing Waveform of Write Cycle (\overline{WE} control) : x16 I/O mode

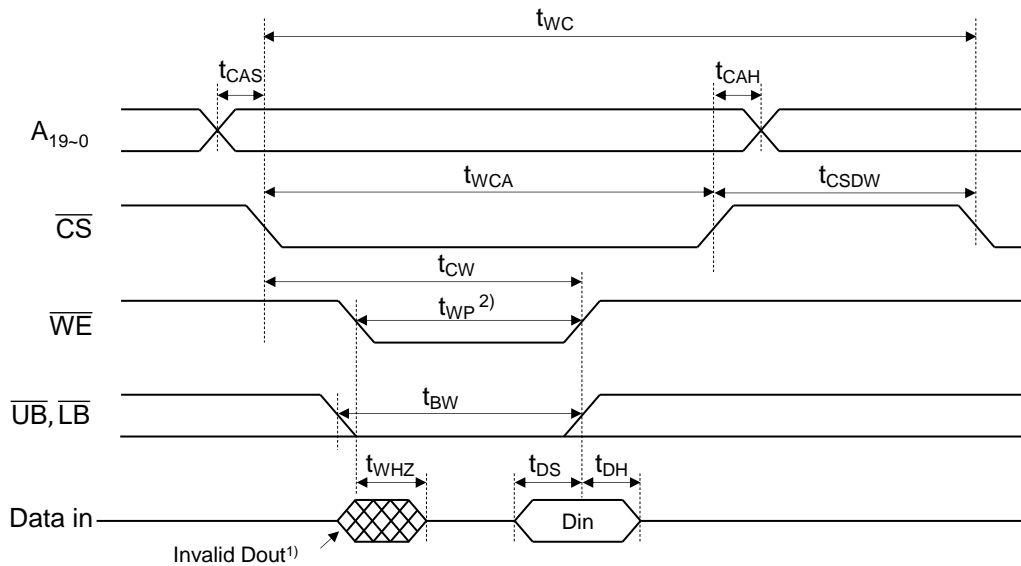
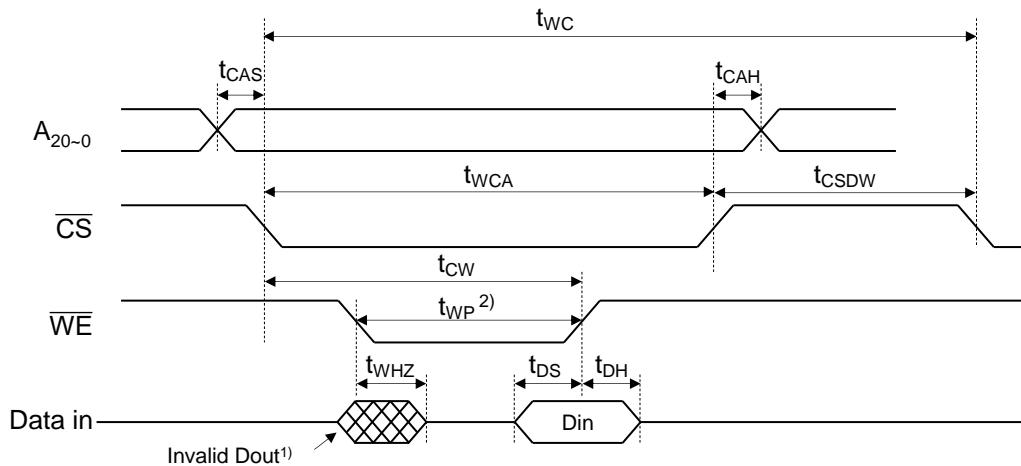


Figure 11 : Timing Waveform of Write Cycle (\overline{WE} control) : x8 I/O mode



Note :

1. The data pins remain in High-Z state if the time of \overline{CS} falling to \overline{WE} falling is smaller than 30ns or \overline{OE} is High.
2. In case that the data pins do not remains in High-Z state, t_{WP} should be t_{WP1}
3. $t_{WCA} + t_{CSDW} \geq t_{WC}$

Write Operation ($\overline{\text{CS}}$ control) : Interpage

Write operation is initiated when $\overline{\text{CS}}$ goes to low and $\overline{\text{WE}}$ is low.

The device latches address on the falling edge of $\overline{\text{CS}}$. It latches the lower byte data on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{LB}}$ and the upper byte data on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{UB}}$ for x16 I/O mode.

It latches the data on the rising edge of $\overline{\text{CS}}$ for x8 I/O mode.

The rising edge of $\overline{\text{CS}}$ causes the device to transfer the input data to memory array.

Figure 12 : Timing Waveform of Write Cycle ($\overline{\text{CS}}$ control) : x16 I/O mode

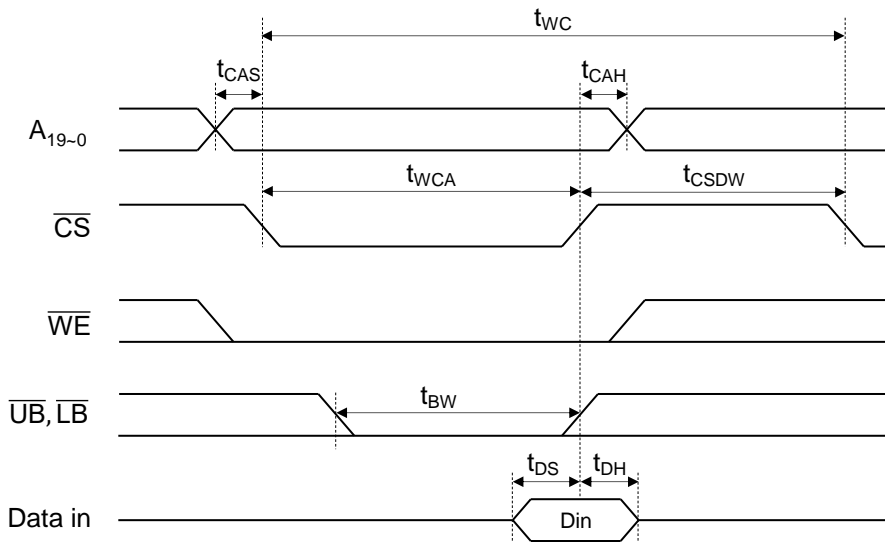
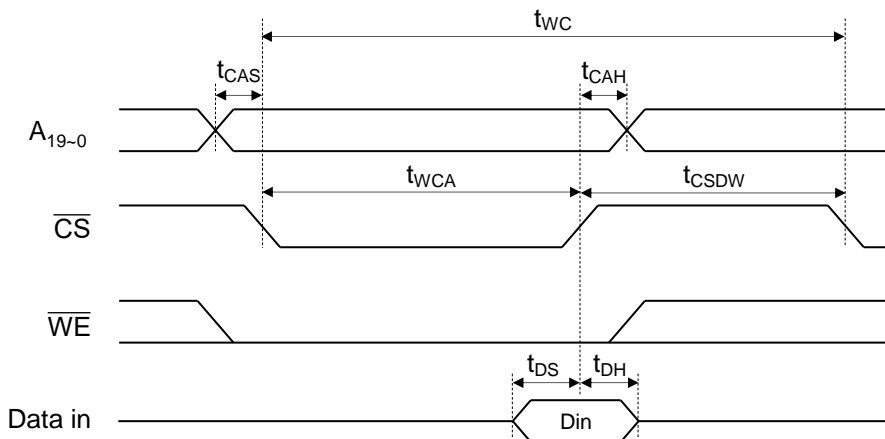


Figure 13 : Timing Waveform of Write Cycle ($\overline{\text{CS}}$ control) : x8 I/O mode



Page Mode Write Operation : Intrapage

The device supports the page mode write function to enhance the write performance.

It latches a page address every falling edge of \overline{WE} . It latches the lower byte data on every rising edge of \overline{WE} or \overline{LB} and the upper byte data on every rising edge of \overline{WE} or \overline{UB} for x16 I/O mode.

It latches the data on every rising edge of \overline{WE} for x8 I/O mode. The rising edge of \overline{CS} causes the device to transfer the input data to memory array. The sequence and length of page address are not restricted. For example, the sequence A2-A0-A1 is available.

Figure 14 : Timing Waveform of Page Mode Write Cycle : x16 I/O Mode

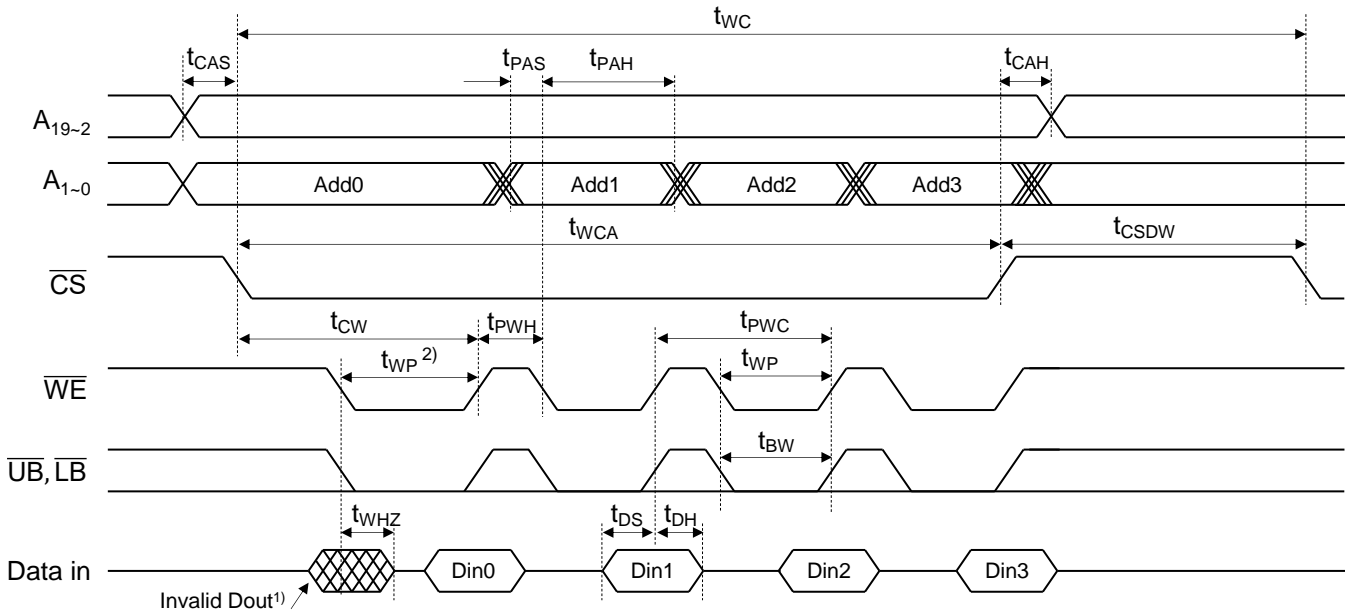
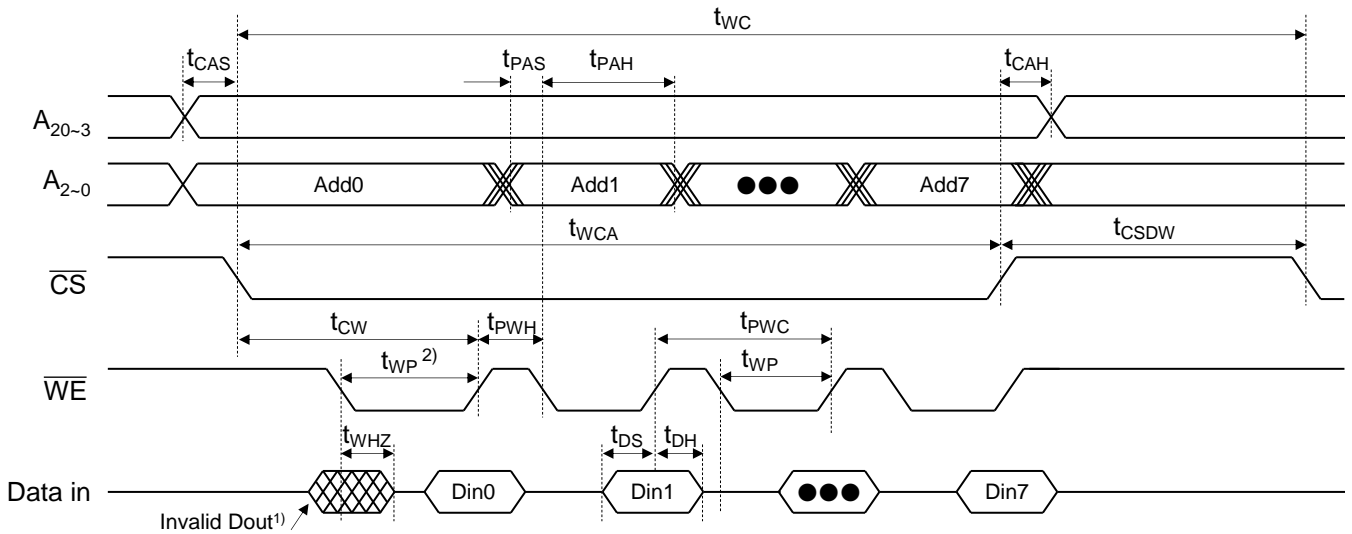


Figure 15 : Timing Waveform of Page Mode Write Cycle : x8 I/O Mode



Note :

- While \overline{CS} is Low, once \overline{WE} goes to Low, output remains in High-Z state even if \overline{WE} goes to High thereafter.

Thermal Resistance

Table 17 : Thermal Resistance

Parameter	Description	48FBGA	54TSOP2	44TSOP2	Unit
θ_{JA}	Thermal resistance (junction to ambient)	69.4	50.3	65.2	°C/W
θ_{JC}	Thermal resistance (junction to case)	31.1	14.4	15.9	

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

Part Numbering System

S	3	R	x	x	x	x	x	x	x	-	x	x	x	x	x	x	x
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Netsol Memory : S

MRAM : 3

Async Parallel Interface : R

Density

1Mb : 10 2Mb : 20
 4Mb : 40 8Mb : 80
 16Mb : 16 32Mb : 32
 64Mb : 64

I/O Organization

x8 : 08
 x16 : 16

VCC

2.70~3.60V : V
 1.71~1.98V : R

CS pin option

1CS pin : 1

Special Code
 by customer request
 Default : 00

Packing Material
 Tray : 0 T&R : T

Speed
 70ns : 70

Temperature
 Commercial : C
 Industrial : I

Package
 44TSOP2 : U
 54TSOP2 : P
 48FBGA : X

Generation
 1st Generation : M

Ordering Part Numbers

Table 18 : Ordering Part Numbers

Density	Org.	Temperature	Package	Packing Material	Part Number
1Mb	x16	-40°C ~ 85°C	44TSOP2	Tray	S3R1016V1M-UI70
				Tape and Reel	S3R1016V1M-UI70T
			48FBGA	Tray	S3R1016V1M-XI70
				Tape and Reel	S3R1016V1M-XI70T
	x8	-40°C ~ 85°C	44TSOP2	Tray	S3R1008V1M-UI70
				Tape and Reel	S3R1008V1M-UI70T
			48FBGA	Tray	S3R1008V1M-XI70
				Tape and Reel	S3R1008V1M-XI70T
2Mb	x16	-40°C ~ 85°C	44TSOP2	Tray	S3R2016V1M-UI70
				Tape and Reel	S3R2016V1M-UI70T
			48FBGA	Tray	S3R2016V1M-XI70
				Tape and Reel	S3R2016V1M-XI70T
	x8	-40°C ~ 85°C	44TSOP2	Tray	S3R2008V1M-UI70
				Tape and Reel	S3R2008V1M-UI70T
			48FBGA	Tray	S3R2008V1M-XI70
				Tape and Reel	S3R2008V1M-XI70T
4Mb	x16	-40°C ~ 85°C	44TSOP2	Tray	S3R4016V1M-UI70
				Tape and Reel	S3R4016V1M-UI70T
			48FBGA	Tray	S3R4016V1M-XI70
				Tape and Reel	S3R4016V1M-XI70T
	x8	-40°C ~ 85°C	44TSOP2	Tray	S3R4008V1M-UI70
				Tape and Reel	S3R4008V1M-UI70T
			48FBGA	Tray	S3R4008V1M-XI70
				Tape and Reel	S3R4008V1M-XI70T
8Mb	x16	-40°C ~ 85°C	54TSOP2	Tray	S3R8016V1M-PI70
				Tape and Reel	S3R8016V1M-PI70T
			48FBGA	Tray	S3R8016V1M-XI70
				Tape and Reel	S3R8016V1M-XI70T
	x8	-40°C ~ 85°C	44TSOP2	Tray	S3R8008V1M-UI70
				Tape and Reel	S3R8008V1M-UI70T
			48FBGA	Tray	S3R8008V1M-XI70
				Tape and Reel	S3R8008V1M-XI70T

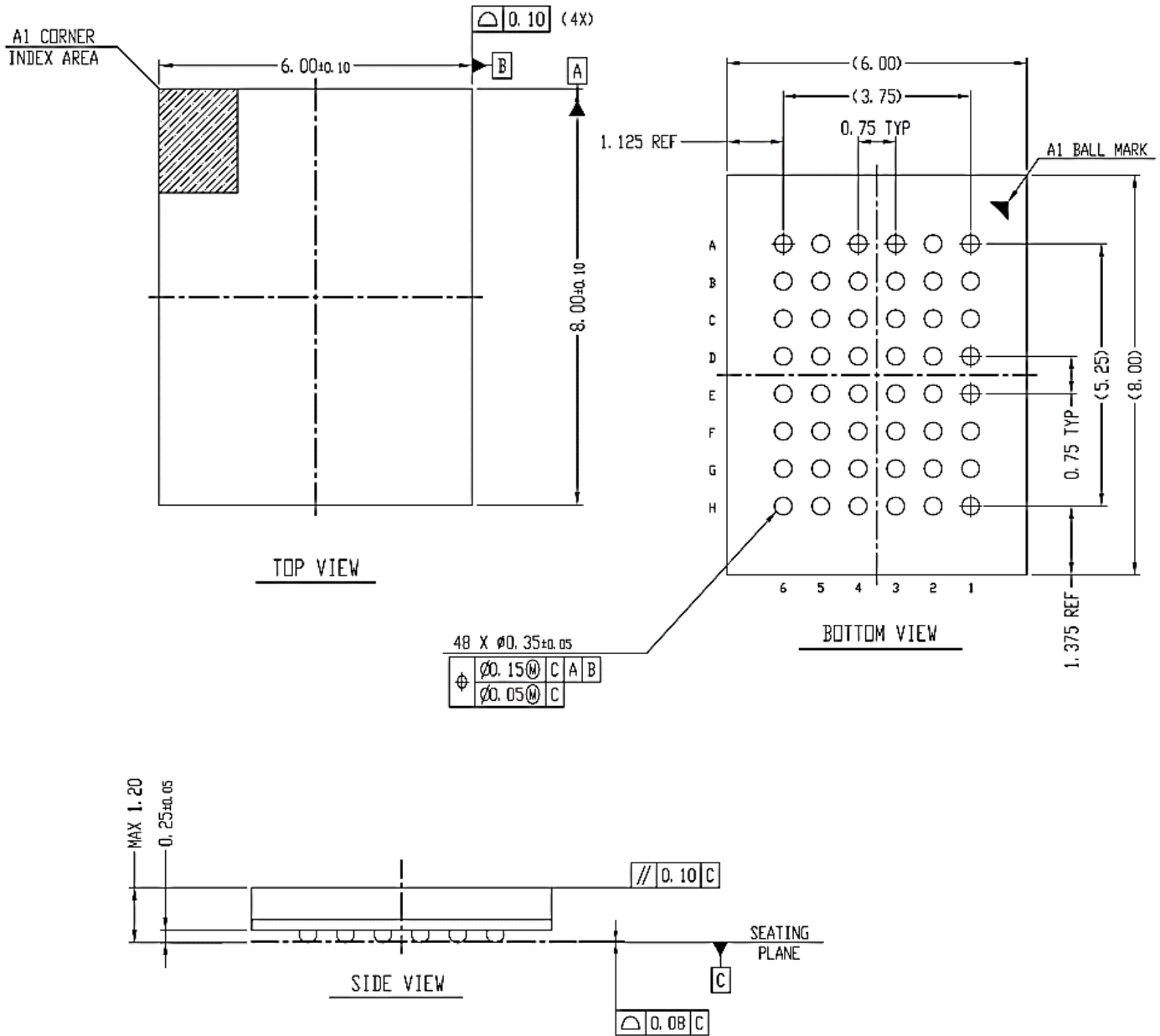
* Continue to next page

Table 18 : Ordering Part Numbers

Density	Org.	Temperature	Package	Packing Material	Part Number
16Mb	x16	-40°C ~ 85°C	54TSOP2	Tray	S3R1616V1M-PI70
				Tape and Reel	S3R1616V1M-PI70T
			48FBGA	Tray	S3R1616V1M-XI70
				Tape and Reel	S3R1616V1M-XI70T
	x8	-40°C ~ 85°C	44TSOP2	Tray	S3R1608V1M-UI70
				Tape and Reel	S3R1608V1M-UI70T
			48FBGA	Tray	S3R1608V1M-XI70
				Tape and Reel	S3R1608V1M-XI70T

Package Dimension

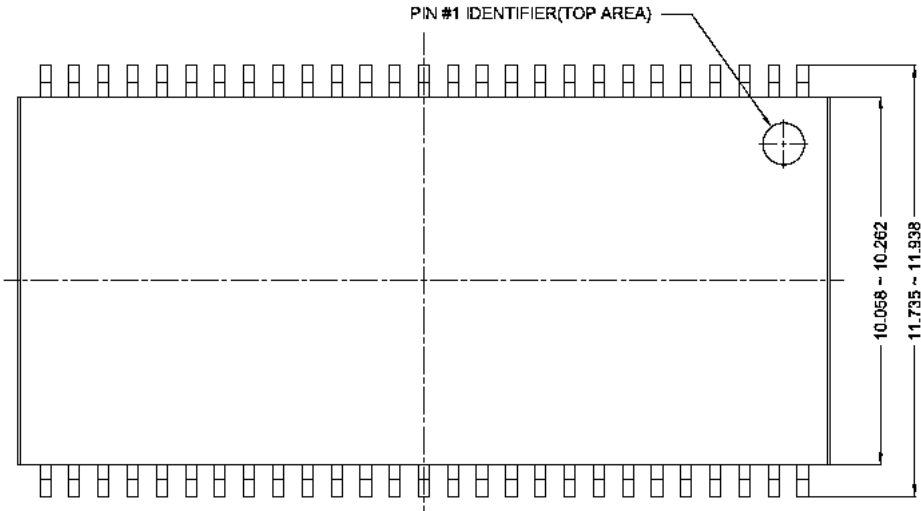
48 FBGA



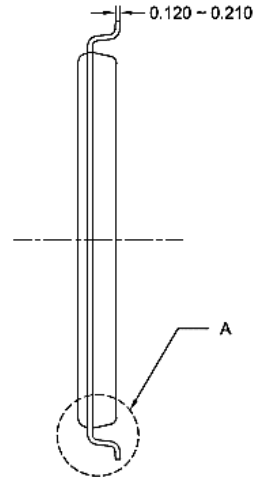
[Notes]

1. All Dimensions in Millimeters
2. Solder ball Diameter is post reflow diameter
(Raw Solder ball size is $\Phi 0.30\text{mm}$)

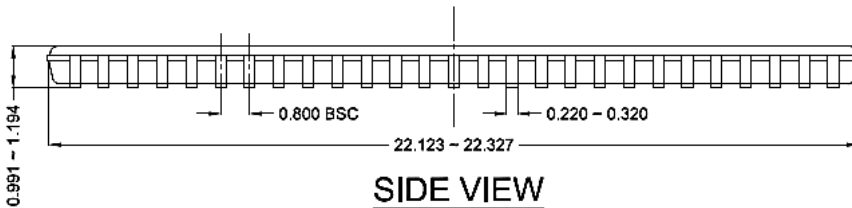
54 TSOP2



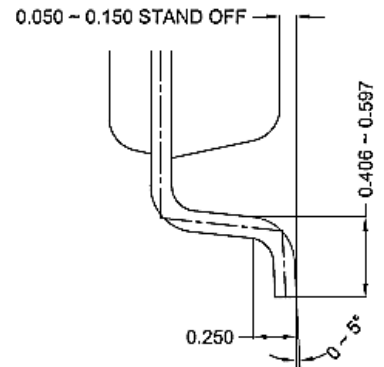
TOP VIEW



SIDE VIEW



SIDE VIEW

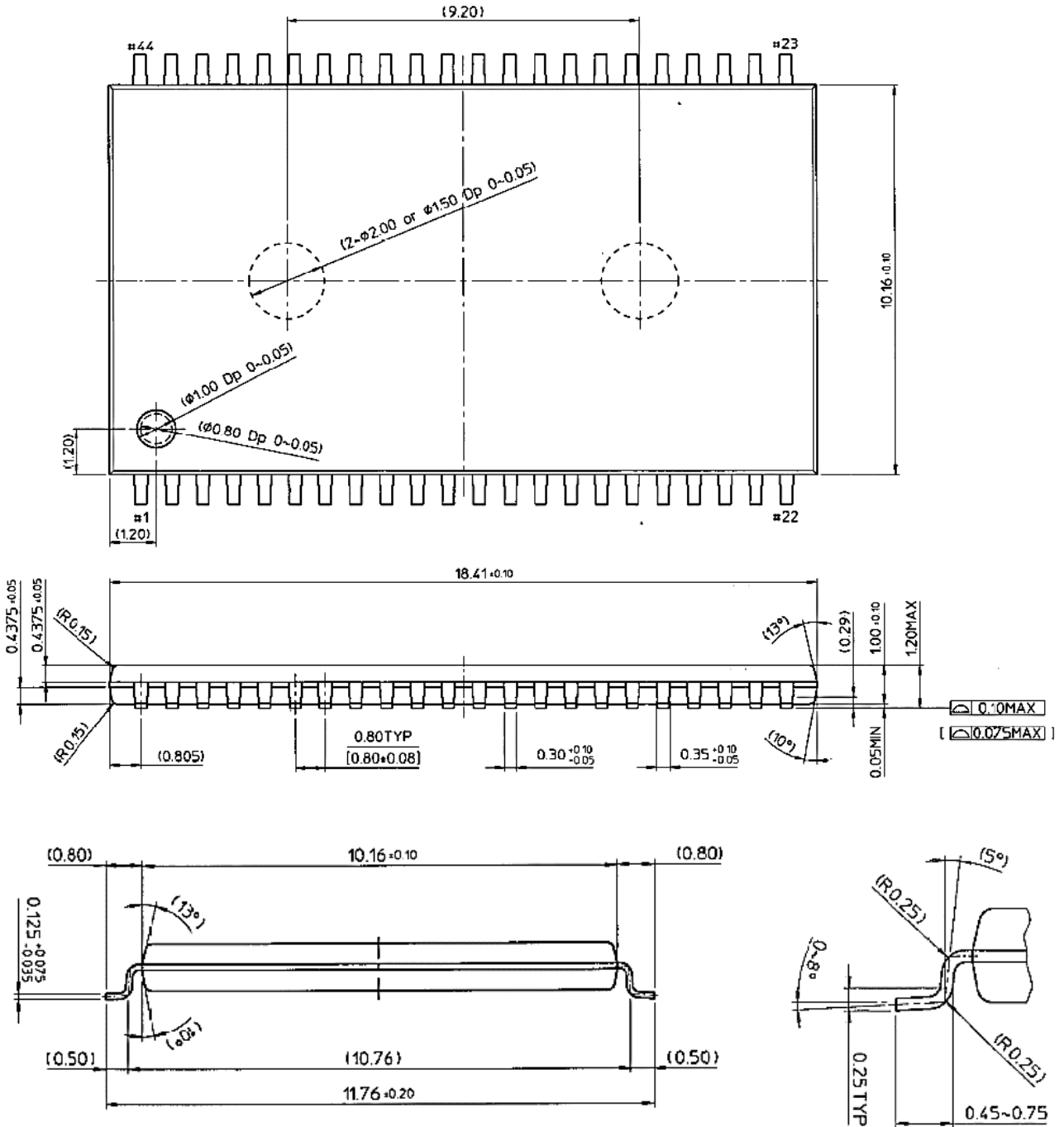


DETAIL "A"

[Notes]

1. Dimensions in Millimeters
2. Lead Finish : Solder Plated
3. Package dimensions refer to JEDEC MS-024

44 TSOP2



[Notes]

1. Dimensions in Millimeters/Inches
2. Lead Finish : Solder Plated
3. Package dimensions refer to JEDEC MS-024

Revision History

Revision	Date	Description
0.1	Jun, 2022	Initial Release, Preliminary
0.2	Jan, 2023	<ol style="list-style-type: none">1. Update the magnetic immunity parameter(Table 9)2. Update the pin capacitance(Table 11)3. Update thermal resistance(Table 17)4. Change Ordering Part Numbers(Table 18)<ul style="list-style-type: none">- delete commercial temperature range